Talks

Corso di Laurea in Elettronica

Functional verification

Guest Lecture at the University of Pisa (Apple)

Egidio Pescari

Digital Verification Manager

APPLE

GIOVEDÌ 20 MAGGIO

h. 14.30

AULA B22 POLO B

ONLINE: https://cutt.ly/Jb0cDXV

In order to save cost and to match time to market, the Functional Verification is one of the activities that assumed a fundamental role in the ASIC development flow.
In the ASIC project development process the majority of effort is spent in functional verification.
The lecture intends to provide an overview of the digital verification flow, languages and methodologies talking about the activity of a DV engineer from the ASIC specification to the Tape Out.

Bio

Egidio is Digital Verification manager at Apple. He graduated in Electronic Engineer at Perugia University in 1998.
He worked as digital designer and verification engineer in Aurelia Microelettronica, Yogitech and Dialog Semiconductor acquiring experience in digital circuit design and specialising in digital verification techniques and methodologies. He joined Apple in 2019.

Link to the Talk

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